

Operational Amplifier

DESCRIPTION

The RH108A is a precision operational amplifier particularly well-suited for high source impedance application-srequiring low offset and bias currents and low power-consumption.

The wafer lots are processed to Linear Technology's inhouse Class S flow to yield circuits usable in stringent-military applications.

For complete electrical specifications, performance curves and applications information, see the LM108A/LM108 data sheet.

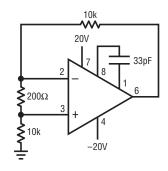
ABSOLUTE MAXIMUM RATINGS

(Note 1)

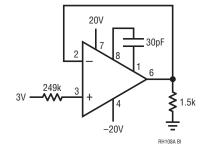
Supply Voltage	±20V
Differential Input Current (Note 1)	±10mA
Input Voltage (Note 2)	±15V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	–55°C to 125°C
Storage Temperature Range	–65°C to 150°C
Lead Temperature (Soldering, 10 se	ec)300°C

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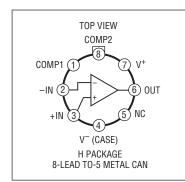
BURN-IN CIRCUIT

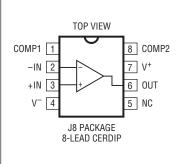


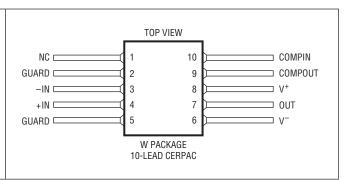
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PACKAGE INFORMATION







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TABLE 1: ELECTRICAL CHARACTERISTICS (Preirradiation, Note 4)

		!		T _A = 25°C			SUB-	-55°C ≤ T _A ≤ 125°C			SUB-	
SYMBOL	PARAMETER	CONDITIONS	NOTES	MIN.	TYP	MAX	GROUP	MIN	TYP	MAX	GROUP	UNITS
V_{0S}	Input Offset Voltage					0.5	1			1.0	2,3	mV
$\frac{\Delta V_{OS}}{\Delta Temp}$	Average Tempco of Offset Voltage		3							5.0		μV/°C
I _{OS}	Input Offset Current					0.2	1			0.4	2,3	nA
$\frac{\Delta I_{S}}{\Delta Temp}$	Average Tempco of Offset Current		3							2.5		pA/°C
I _B	Input Bias Current					2.0	1			3.0	2,3	nA
A _{VOL}	Large-Signal Voltage Gain	$V_S = \pm 15V, V_{OUT} = \pm 10V$ $R_L \ge 10k$		80			4	40			5,6	V/mV
CMRR	Common Mode Rejection Ratio			96			1	96			2,3	dB
PSRR	Power Supply Rejection Ratio			96			1	96			2,3	dB
	Input Voltage Range	$V_S = \pm 15V$	3	±13.5				±13.5				V
V _{OUT}	Output Voltage Swing	$V_S = \pm 15V, R_L = 10k$		±13			4	±13			5,6	V
R _{IN}	Input Resistance		3	30								MΩ
I _S	Supply Current	(Note 6)				0.6	1			0.4	2	mA

TABLE 1A: ELECTRICAL CHARACTERISTICS (Preirradiation, Note 4)

SYMBOL	PARAMETER	CONDITIONS	NOTES	10KRA MIN	D (Si) Max	20KRA Min	D (Si) Max	50KRA MIN	D (Si) Max	80KRA Min	D (Si) Max	UNITS
V _{OS}	Input Offset Voltage				0.5		0.5		0.5		1.0	mV
I _{OS}	Input Offset Current				0.3		0.3		0.3		0.3	nA
I _B	Input Bias Current				±2.0		±2.0		±2.0		±4.0	nA
A _{VOL}	Large-Signal Voltage Gain	$V_S = \pm 15V, V_{OUT} = \pm 10V$ $R_L \ge 10k$		98		98		90		86		dB
CMRR	Common Mode Rejection Ratio			96		96		84		70		dB
PSRR	Power Supply Rejection Ratio		4	96		96		84		70		dB
	Input Voltage Range		3	±13.5		±13.5		±13.5		±13.5		V
V _{OUT}	Output Voltage Swing			±13		±13		±13		±13		V
R _{IN}	Input Resistance		3	30		30		30		30		MΩ
Is	Supply Current				0.6		0.6		0.6		0.6	mA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: For supply voltages less than ± 15 V, the maximum input voltage is equal to the supply voltage.

Note 3: Guaranteed by design, characterization or correlation to othertested parameters.

Note 4: $\pm 5V \le V_S \le \pm 20V$ preirradiation, $\pm 5V \le V_S \le \pm 15V$ postirradiation, unless otherwise noted.

Note 5: $V_S = \pm 15 V$, $V_{CM} = 0 V$, $T_A = 25 ^{\circ} C$ unless otherwise noted.

Note 6: $25^{\circ}C \le T_A \le 125^{\circ}C$.

TECHNOLOGY TECHNOLOGY

TABLE 2: ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUP
Final Electrical Test Requirements (Method 5004)	1*,2,3,4,5,6
Group A Test Requirements (Method 5005)	1,2,3,4,5,6
Group C and D End Point Electrical Parameters (Method 5005)	1

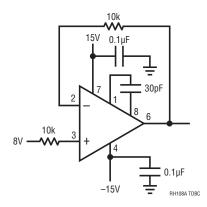
^{*}PDA applies to subgroup 1. See PDA Test Notes.

PDA Test Notes

The PDA is specified as 5% based on failures from group A, subgroup 1, tests after cooldown as the final electrical test in accordance with method 5004 of MIL-STD-883 Class B. The verified failures (including Delta parameters) of group A, subgroup 1, after burn-in divided by the total number of devices submitted for burn-in in that lot shall be used to determine the percent for the lot.

Linear Technology Corporation reserves the right to test to tighter limits than those given.

TOTAL DOSE BIAS CIRCUIT



REVISION HISTORY (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
С	11/10	Note 4 revised and added to Power Supply Rejection Ratio.	2



TYPICAL PERFORMANCE CHARACTERISTICS

